What Is Claimed Is:

1. A driving circuit for a flat panel display comprising:

a latch unit which is applied a control signal from a shift register to sequentially sample N-bit digital picture signals and to store the picture signals, and simultaneously output the sampled picture signals by a line pass signal; and

a voltage to current converting unit distributing an outer reference current to a plurality of paths using a current mirror method, and supplying current of different levels to data lines of the display panel according to logical combinations of the picture signals which are applied from the latch unit.

2. The circuit of claim 1, wherein the latch unit comprises:

a first latch unit being applied the control signal from the shift register to sample and store a digital picture signal having a plurality of bit numbers; and

a second latch unit outputting the digital picture signal sampled in the first latch unit simultaneously according to an outer line-pass signal.

3. The circuit of claim 1, wherein the shift register, the latch unit and the voltage to current converting unit are formed

in the display panel.

4. The circuit of claim 1, wherein the display panel is an organic electroluminescence display panel.

5. The circuit of claim 1, wherein the voltage to current converting unit comprises:

a first switching unit for controlling a flow of a reference current by an enable signal;

a second switching unit connected to the first switching unit for controlling the flow of the reference signal by the enable signal;

a first NMOS transistor for forming a reference path on which the reference current flows between the first switching unit and ground by being applied the reference current on a gate electrode thereof;

a plurality of NMOS transistors not including the first NMOS transistor for forming a plurality of current paths in a parallel direction between the data line and the ground of the display panel according to picture signals having a plurality of bit numbers by being applied the reference signal on respective gate electrodes thereof; and

a plurality of switching units for controlling switching

of the plurality of current paths by being applied the picture signal having the plurality of bit numbers independently.

6. The circuit of claim 5, wherein the first NMOS transistor and the plurality of NMOS transistors are poly-crystalline silicon thin film transistors (TFTs).

7. The circuit of claim 5, wherein the first switching unit, second switching unit and the plurality of switching units comprise NMOS transistors.

8. The circuit of claim 7, wherein each NMOS transistor is a poly-crystalline silicon TFT.

9. The circuit of claim 5 further comprising a capacitor connected between the second switching unit and ground for charging the reference current.

10. The circuit of claim 5, wherein the plurality of NMOS transistors includes an NMOS transistor for resetting the gate electrodes of the first NMOS transistor which forms the reference path and of the plurality of NMOS transistors which form the plurality of current paths in a parallel direction to ground

potential by a reset signal.

11. The circuit of claim 5, wherein the plurality of paths are formed to be the same as the bit numbers of the picture signal.

12. The circuit of claim 5, wherein the plurality of paths are formed to be the same as the number of logical combinations of the bits in the picture signal.

13. The circuit of claim 5, wherein the first NMOS transistor is formed to have a ratio of channel width/length differently from those of the plurality of NMOS transistors.

14. The circuit of claim 13, wherein the ratios of channel widths/lengths of the plural NMOS transistors are made to be different from those of each other.

15. The circuit of claim 13, wherein the ratios of channel widths/lengths of the plurality NMOS transistors are made to be the same as each other.